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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/061,066	01/29/2002	Adrian Stoica	NPO-20773-1-CU	7632

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EXAMINER	
LUU, CUONG V	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/061,066	STOICA, ADRIAN	
	Examiner	Art Unit	
	Cuong V. Luu	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/29/02, 3/24/02*. 8/20/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-27 have been examined. Claims 1-27 have been rejected.

Claim Objections

1. Claim 18 is objected to because of the following informality: there is a grammatical error in clause "wherein each candidate circuit is been modeled". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7, 15-27 are rejected under 35 U.S.C. 102(b) as being unpatentable by Stoica et al (Evolutionary Design of Electronic Devices and Circuits, Evolutionary Computation, 1999. IEEE CEC 99, July 1999).

2. As per claim 1, Stoica et al teach a method of evolving a circuit from plural candidate circuits, comprising:

assigning each one of a plurality configurable circuit models of different levels of model resolutions to different individual ones of at least subset of said plural candidate circuits (p. 1272, col. 1, lines 4-9, and col. 2, lines 28-35. SPICE simulation software has many levels of models for transistors for different levels of resolution or accuracy and different fabrication manufacturers. Therefore, depending on interest in level of accuracy, a model is assigned to one or more or all transistors or in a circuit. As a result, the examiner interprets that assigning different levels of model resolution to different circuits inherits from SPICE).

producing a simulation model for each one of at least said subset of said candidate circuits by configuring configurable model assigned to the one candidate circuit accordance with the one candidate circuit, whereby to produce plurality of simulation models corresponding to at least said subset said candidate circuits whose resolutions are distributed among said different levels model resolutions (p. 1272, col. 1, paragraph 1, lines 4-9);

obtaining from each simulation model fitness function the corresponding candidate circuit (p. 1274, col. 1, lines 5-6);

ranking said candidate circuits in accordance said fitness functions (p. 1272, col. 1, lines 7-9);

changing assignments of candidate circuits among said configurable circuit models (p. 1272, col. 1, lines 14-16);

repeating the steps of producing, obtaining and ranking, whereby to perform them in successive iterations (p. 1272, col. 1, lines 14-16).

3. As per claim 2, Stoica et al step of eliminating candidate circuits corresponding to inferior ranking (p. 1272, Fig. 2. In the flow chart of Fig. 2, the box of "select the best" is interpreted as eliminating circuits of inferior ranking).

4. As per claim 3, Stoica et al teach ranking step is followed by a step of adding another of said candidate circuits to said subset candidate circuits (p. 1272, col.1, lines 4-16).

5. As per claim 4, Stoica et al teach the step of assigning is carried out by randomly assigning ones of said plural configurable models to ones of said plural candidate circuits (p.1274, col. 2, lines 29-31; p. 1275, col. 1, line 1-2. The examiner interprets "genetic algorithm is expected to obtain the optimal parameter set" as randomly assigning parameters to candidate circuit and evolving those parameters according genetic algorithm to select the optimal set for parameters, and parameters of device(s) determine models for device(s)).

6. As per claim 5, Stoica et al teach using SPICE to simulate a candidate circuit and assigning each candidate circuit with a different model as discussed in claim 1. SPICE has a finite number of levels of model. Therefore, all different models of resolution have to be assigned to candidate circuits within a finite number of iterations. These limitations are, therefore, rejected.

7. As per claim 6, this limitation is included in the process of eliminating the inferior ranked circuit as discussed in claim 2. It is, therefore, rejected.

8. As per claim 7, these limitations have already been discussed in claim 2. They are, therefore, rejected for the same reasons.

9. As per claim 15, Stoica et al teach a method of evolving a circuit comprising modeling plural candidate circuits with a heterogeneous mix of models of different levels of resolution (p. 1272, col. 1, lines 14-16, and col. 2, lines 28-35. SPICE simulation software has many levels of models for transistors for different levels of resolution or accuracy and different fabrication manufacturers. Therefore, depending on interest in level of accuracy, a model is assigned to one or more or all transistors or in a circuit. As a result, the examiner interprets that assigning different levels of model resolution to different circuits inherits from SPICE).

10. As per claim 16, these limitations have already been discussed in claims 15 and 8. They are, therefore, rejected for the same reasons.

11. As per claim 17, these limitations have already been discussed in claims 1 and 5. They are, therefore, rejected for the same reasons.

12. As per claim 18, this limitation has already been discussed in claim 5. It is, therefore, rejected for the same reasons.

13. As per claim 19, assigning resolution level model to a circuit is a matter of choice. All candidate circuits are not required to be assigned to a different resolution level model at each iteration in order for the method to work. This limitation is, therefore, rejected.

14. As per claim 20, this limitation has already been discussed in claim 5. It is, therefore, rejected for the same reasons.

15. As per claim 21, these limitations have already been discussed in claim 1. They are, therefore, rejected for the same reasons.

16. As per claim 22, these limitations have already been discussed in claim 2. They are, therefore, rejected for the same reasons.

17. As per claim 23, these limitations have already been discussed in claim 3. They are, therefore, rejected for the same reasons.

18. As per claim 24, these limitations have already been discussed in claim 4. They are, therefore, rejected for the same reasons.

19. As per claim 25, these limitations have already been discussed in claim 5. They are, therefore, rejected for the same reasons.

20. As per claim 26, these limitations have already been discussed in claim 6. They are, therefore, rejected for the same reasons.

21. As per claim 27, these limitations have already been discussed in claim 7. They are, therefore, rejected for the same reasons.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 8-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stoica et al (Evolutionary Design of Electronic Devices and Circuits, Evolutionary Computation, 1999. IEEE CEC 99, July 1999), and further in view of Koza et al (Automated Synthesis of Computational Circuits Using Genetic Programming, 13-16 April 1997, Evolutionary Computation, 1997, IEEE International Conference).

22. As per claim 8, Stoica et al teach a method of evolving a circuit from plural candidate circuits, comprising:

assigning every one plurality of configurable circuit models of different levels of model resolutions to each one of at least a subset of said plural candidate circuits (p. 1272, col. 1, lines 4-9, and col. 2, lines 28-35. SPICE simulation software has many levels of models for transistors for different levels of resolution or accuracy and different fabrication manufacturers. Therefore, depending on interest in level of accuracy, a model is assigned to one or more or all transistors or in a circuit. As a result, the examiner interprets that assigning different levels of model resolution to different circuits inherits from SPICE);

producing plural simulation models for each one of at least set subset of said candidate circuits by configuring each configurable model in accordance with the one candidate circuit, whereby to produce a plurality of simulation models for each candidate circuit (p. 1272, col. 1, lines 4-9);

ranking said candidate circuits in accordance with their fitness functions (p. 1272, col. 1, lines 7-9).

obtaining from the plurality of simulation models of each candidate circuit a plurality fitness functions of the corresponding candidate circuit,

but do not teach combining said plurality of fitness functions into a single fitness function of the one candidate circuit;

Koza et al teach combining said plurality of fitness functions into a single fitness function of the one candidate circuit (p. 449, col. 1, lines 51-61, and col. 2, line 1).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Stoica et al and Koza et al. Koza et al's teaching of combining said plurality of fitness functions into a single fitness function of the one candidate circuit would have helped create fitness functions for candidate circuits over different

resolution models to obtain better performance evaluation of candidate circuits over a range of models.

23. As per claim 9, Stoica et al teach plural configurable models constitute three models corresponding to three different levels of resolution (p. 1272, col. 2, lines 28-35. SPICE has 3 basic levels of resolution for MOS transistor).

24. As per claim 10, Stoica et al teach plural configurable models constitute two models corresponding to two different levels of resolution (p. 1272, col. 2, lines 28-35. SPICE has 3 basic levels of resolution for MOS transistor two of which can correspond to two levels of resolution mentioned in this limitation).

25. As per claim 11, this limitation has already been discussed in claim 2. It is, therefore, rejected for the same reasons.

26. As per claim 12, this limitation has already been discussed in claim 3. It is, therefore, rejected for the same reasons

27. As per claim 13, Koza et al teach the step of combining said fitness functions comprises forming an average of said functions (p. 449, col. 1, lines 51-61, and col. 2, line 1).

28. As per claim 14, Koza et al teach said average is a weighted average (p. 449, col. 1, lines 51-61, and col. 2, line 1).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cuong V. Luu whose telephone number is 571-272-8572. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere, can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. An inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CVL

Thai Phan
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